

JUN 01 2007

Patent EMC-01-018
U.S.S.N.: 09/933,468REMARKS

In response to the final Office Action mailed February 1, 2007, applicant respectfully requests reconsideration. In the Office Action, claims 1-24 were rejected. Claims 1-24 remain pending in the application.

Claim Rejections Under 35 U.S.C. §102

Claims 1, 2, 6-8, 13, 14 and 18-20 were rejected under 35 U.S.C. §102(b) as being anticipated by Jamal (US-5,572,712). This rejection is respectfully traversed, as Jamal does not teach every element recited in claims 1, 2, 13 and 14, as is required for a proper rejection under 35 U.S.C. §102(b).

Independent claim 1 recites, among other features, that the third logic section selectively couples the first logic section or the second logic section to the SUT based upon respective states of *two control signals*, one of the two control signals being transmitted to the third logic section from a source that is external to the SUT, the first logic section, the second logic section, and the third logic section, the *other* of the two control signals being transmitted to the third logic section *from the first logic section*.

The examiner takes the position that Jamal teaches two control signals, the first being the test mode enable signal, which is input to the initial logic device 46, and the other being a control signal from clock and control signal generator 52 to the multiplexer 44.

However, Jamal's system has only *one control signal* for determining which of the "other components" and the BIST circuit 40 will be coupled to the RAM 42. As set forth in Column 5, lines 15-20, in a "normal" or "functional" mode, the "other components" and the RAM 42 interact through the multiplexer 44, which detaches the BIST 40 from the RAM 42 during the normal mode. The test mode signal applied to the initialization logic 46 activates the BIST 40 (Col. 5, lines 21-22). Further, the initialization logic 46 commands the multiplexer 44 to decouple the RAM 42 from the other components of the integrated circuit die 32 and then couples the BIST 40 to the RAM (Col. 5, lines 23-25). The logic 46, based on the input of the test mode signal, *activates* the address generator 48, the MISR 50 and the clock and control signal

generator 52 (Col. 5, lines 23-28). Therefore, without the input of the test mode signal to logic 46, the BIST 40 is *inactive*, and therefore does not output *any* signals to the multiplexer 44.

While the examiner states that Jamal discloses a control signal from clock and control signal generator 52 (which the examiner states corresponds to applicant's claimed "first logic device") to the multiplexer 44, this is simply not the case. As set forth in Column 5, lines 35-38, the generator 52 generates internal clock signals, address direction signals, read/write enable signals, MISR clock signals, test patterns, and an end-of-test signal for the RAM 42. Therefore, the generator 52 *does not generate or input a control signal to the multiplexer 44*. In fact, "the clock and control signal generator 52 generates the BIST test patterns and transfers them to the RAM 42 undergoing test through the multiplexer logic 44." (Column 5, lines 39-41). These are the only inputs from the generator 52 to the multiplexer 44.

Based on the foregoing, it is clear that Jamal teaches a *single control signal*, the "test mode" signal input to the initial logic 46, which determines which of the "other components" and the BIST 40 are coupled to the RAM 42. When the test mode signal is "low", the "other components" are coupled to the RAM 42 through multiplexer 44 and when the test mode signal is "high", the BIST 40 is coupled to the RAM 42 through multiplexer 44.

Accordingly, since Jamal does not teach every element recited in independent claim 1, independent claim 1 is allowable over Jamal and the rejection of independent claim 1 under 35 U.S.C. §102(b) should be withdrawn.

Claims 2 and 6-8 depend on independent claim 1 and are allowable for at least the same reasons as independent claim 1.

Applicant further asserts that, based on Jamal's specific description of the need for only one control signal, as described above, there is no suggestion or motivation to modify Jamal to include a second control signal. In fact, based on Jamal's specific description of the need for only one control signal, Jamal actually *teaches away* from anything other than a single control signal.

Independent claim 6 recites, among other features, selectively coupling the first logic section or the second logic section to the SUT based upon respective states of *two*

Patent EMC-01-018
U.S.S.N.: 09/933,468

control signals, one of the two control signals being transmitted to the third logic section from a source that is external to the SUT, the first logic section, the second logic section, and the third logic section, the *other* of the two control signals being transmitted to the third logic section *from the first logic section*.

Based on the argument set forth above, since Jamal does not teach two control signals, Jamal does not teach every element recited in independent claim 6. Accordingly, independent claim 6 is allowable over Jamal and the rejection of independent claim 6 under 35 U.S.C. §102(b) should be withdrawn.

Claims 14 and 18-20 depend on independent claim 6 and are allowable for at least the same reasons as independent claim 6.

Claim Rejections Under 35 U.S.C. §103

Claims 3-5, 9-12, 15-17, 21-24 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jamal by itself and in separate combinations with Miner and Walker. This rejection is respectfully traversed, as the modification to Jamal suggested by the examiner, as well as the combinations suggested by the examiner, do not teach the invention recited in the claims.

Independent claim 10 recites, among other features, selectively coupl[ing] the first logic section or the respective second logic section to a respective system-under-test based upon a respective control signal from the first logic section and also based upon another control signal, the another control signal being transmitted to each third logic section from a source that is external to the plurality of systems-under-test, the first logic section, the plurality of second logic sections, and the plurality of third logic sections.

Based on the argument set forth above, since Jamal does not teach two control signals, the modification of Jamal suggested by the examiner does not teach or suggest the invention recited in independent claim 10. Accordingly, independent claim 10 is allowable over Jamal and the rejection of independent claim 10 under 35 U.S.C. §103(a) should be withdrawn.

Claims 11 and 12 depend on independent claim 10 and are allowable for at least the same reasons as independent claim 10.

Patent EMC-01-018
U.S.S.N.: 09/933,468

Independent claim 22 recites, among other features, selectively coupl[ing] the first logic section or the respective second logic section to a respective system-under-test based upon a respective control signal from the first logic section and also based upon another control signal, the another control signal being transmitted to each third logic section from a source that is external to the plurality of systems-under-test, the first logic section, the plurality of second logic sections, and the plurality of third logic sections.

Based on the argument set forth above, since Jamal does not teach two control signals, the combination of Jamal and Miner suggested by the examiner does not teach or suggest the invention recited in independent claim 22. Accordingly, independent claim 22 is allowable over Jamal and the rejection of independent claim 22 under 35 U.S.C. §103(a) should be withdrawn.

Claims 23 and 24 depend on independent claim 10 and are allowable for at least the same reasons as independent claim 10.

Based on the foregoing, applicants respectfully assert that claims 1-24 are allowable over the art of record and respectfully request that a timely Notice of Allowance be issued in this application.

In the event the Patent Office deems personal contact desirable in disposition of this matter, the Office is invited to contact the undersigned attorney at (508) 293-7835.

Please charge any fees occasioned by this submission to Deposit Account No. 05-0889.

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Respectfully submitted,



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